University Program Software Selection

Level One

Product
Conformal - GXL
Conformal Constraint Design - L
Conformal Constraint Design - XL
CCD Multi-Constraint Check option
Conformal Low Power - XL
Conformal Low Power GXL
Conformal ECO Designer

Product
Virtuoso® Quantus QRC Extraction - XL
Virtuoso® Quantus QRC Advanced Analysis GXL Option
Cadence® Quantus QRC Advanced Modeling GXL Option
Cadence® Quantus QRC Display Technology Option
Cadence® Quantus QRC Advanced Modeling20 GXL Option
Cadence® Quantus QRC Advanced Node Modeling Option

Product
Genus Synthesis Solution
Genus Low Power Option
Genus Physical Option
Genus CPU Accelerator Option Partitioned Simulator

Product
Virtuoso® Simulation Environment
Virtuoso® AMS Designer Environment
Virtuoso® Analog Design Environment – XL
Virtuoso® Analog Design Environment – GXL
Virtuoso® Visualization & Analysis XL
Virtuoso® Implementation Aware Design Option
Virtuoso® Layout Suite EAD
Virtuoso® ADE Explorer
Virtuoso® ADE Assembler
Virtuoso® Variation Option
Virtuoso® ADE Verifier
Virtuoso® Schematic Editor HSPICE Interface
Virtuoso® analog HSPICE HSPICE Interface
University Program Software Selection

Product

- Cadence® Framework Integration Runtime Option
- Cadence® SKILL Development Environment
- Virtuoso® Schematic VHDL Interface
- Virtuoso® Schematic Editor Verilog Interface
- Virtuoso® Schematic Editor – XL
- Virtuoso® Analog Oasis Run-Time Option
- Cadence® OASIS for RFDE
- Virtuoso® EDIF 200 Reader
- Virtuoso® EDIF 200 Writer
- Cadence® Design Framework Integrator’s Toolkit
- Dracula® Graphical User Interface
- Dracula® Physical Verification and Extractor Suite
- Diva® Physical Verification and Extractor Suite
- Virtuoso® Layout Suite - GXL
- Virtuoso® DFM Option
- Voltus-Fi Custom Power Integrity Solution - XL
- Virtuoso® Stacked Die Option
- Virtuoso® System Design Platform

Product

- Virtuoso® Advanced Node Framework

Product

- Verifault – XL Simulator
- Verifault – XL Slave Node License
- Incisive™ Enterprise Simulator - XL
- Enterprise Simulator - XL Interface for MTI
- Enterprise Simulator - XL Interface for VCS
- Incisive™ Formal Verifier
- Digital Mixed Signal Option to IES
- Incisive Functional Safety Simulator
- Incisive™ Advanced Option
- Incisive™ Low-Power Simulation Option
University Program Software Selection

Product
Virtuoso® Digital Implementation
Innovus 20/16/14nm Option
Innovus Mixed Signal Option
Innovus High Frequency Route Option
Innovus Hierarchical Design Option
Innovus CPU Accelerator Option
Innovus Implementation System

Product
JasperGold Interactive Option
JasperGold Formal Property Verification APP
JasperGold X-Propagation Verification APP
JasperGold Connectivity Verification APP
JasperGold Coverage APP Option
JasperGold CSR Verification APP
JasperGold Formal Property Verification APP
JasperGold X-Propagation Verification APP
JasperGold Connectivity Verification APP
JasperGold CSR Verification APP
JasperGold Automatic Formal Linting App
JasperGold Coverage Unreachability App
JasperGold Sequential Equivalency Checking APP

Product
Joules RTL Power Solution

Product
Virtuoso® Liberate Server
Virtuoso® Liberate Client
Virtuoso® Liberate LV Server
Virtuoso® Liberate LV Client

Product
vManager Project Server
vManager Linux Client
University Program Software Selection

Product

Modus ATPG
Modus DFT Option
Modus Hierarchical Option

Product

Virtuoso® LDE analyzer Option
Innovus DFM Option
Litho Physical Analyzer
Distributed Process for 8 CPUs
Litho Electrical Analyzer
Cadence® Litho Hotspot Fixing Option

Product

Pcell Generator
Graphical Technology Editor
Generator for Assura™ compatible verification decks
Generator for Diva® compatible verification decks
Error Cell Generator

Product

Cadence® QuickView Layout and Mask Data Viewer
Cadence® QuickView Layout Data Viewer
Cadence® QuickView Sign-off Data Analysis Environment
Cadence® Physical Verification System Design Rule Checker XL
Cadence® Physical Verification System Layout vs. Schematic Checker XL
Cadence® Physical Verification System Programmable Electrical Checker
Cadence® Physical Verification System Programmable Electrical Checker XL
Cadence® Physical Verification System Results Manager
Cadence® Physical Verification System Design Analysis Option
Cadence® Physical Verification System QuickView Signoff Environment
Cadence® Physical Verification System Constraint Validator
Cadence® Physical Verification System Constraint Validator XL
Cadence® Physical Verification System Advanced Device Option
Cadence® Physical Verification System Advanced Analysis Option
Cadence® Physical Verification System Pattern Matching Option
Cadence® Physical Verification System Mask Rule Check Option
Virtuoso® Integrated Physical Verification System Option for Layout Suite
University Program Software Selection

Product

Allegro® Sigrity SI Base
Allegro® Sigrity Power Aware SI Option
Allegro® Sigrity System Serial Link Option
Allegro® Sigrity Package Assessment and Extraction Option
Allegro® Sigrity PKG-PCB SSO Voltus Suite

Product

Allegro® PCB Designer
Allegro® PCB High-Speed Option
Allegro® PCB Miniaturization Option
Allegro® PCB Team Design Option
Allegro® PCB Analog/RF Option
Allegro® PCB Design Planning Option
Allegro® Sigrity PI Base
Allegro® Design Authoring High-Speed Option
Allegro® Design Authoring Multi-Style Option
Allegro® Design Authoring Team Design Option
Cadence® 3D Design Viewer
Allegro® PCB Routing Option
Allegro® PCB Librarian - XL
Allegro® Physical Viewer
Allegro® 2 FPGA System Planner Option
Allegro® ASIC Prototyping with FPGA’s
Cadence® SiP Layout – XL
Allegro® AMS Simulator
Allegro® Pspice Systems Option
Allegro® PCB Symphony Team Design Option
OrbitIO

Product

Virtuoso® Multi-mode Simulation Power Option
Virtuoso® Multi-mode Simulation CPU Accelerator option
Virtuoso® RelXpert
Spectre Extensive Partitioned Simulator
Spectre Characterization Simulator Option
University Program Software Selection

**Product**

Spectre AMS Designer
Spectre Multi-Mode Simulation with AMS

**Product**

Tempus Timing Signoff Solution – L
Tempus Timing Signoff Solution – XL
Tempus Timing Signoff Solution TSO
Tempus Timing Signoff Solution MP
Voltus IC Power Integrity Solution-XL (VTS-XL)
Voltus IC Power Integrity Solution Adv Analysis GXL Option (VTS-AA)

**Product**

Stratus HLS - XL

**Product**

Xcelium Single Core
Xcelium Digital Mixed Signal Option
Cadence® Simulation Analysis Environment (SimVision)
Indago Embedded Software Debug App
University Program Software Selection

Level Two

Product

Allegro® Sigrity SI Base
Allegro® Sigrity Power Aware SI Option
Allegro® Sigrity System Serial Link Option
Allegro® Sigrity Package Assessment and Extraction Option
Allegro® Sigrity PKG-PCB SSO Voltus Suite

Product

Allegro® PCB Designer
Allegro® PCB High-Speed Option
Allegro® PCB Miniaturization Option
Allegro® PCB Team Design Option
Allegro® PCB Analog/RF Option
Allegro® PCB Design Planning Option
Allegro® Sigrity PI Base
Allegro® Design Authoring High-Speed Option
Allegro® Design Authoring Multi-Style Option
Allegro® Design Authoring Team Design Option
Cadence® 3D Design Viewer
Allegro® PCB Routing Option
Allegro® PCB Librarian - XL
Allegro® Physical Viewer
Allegro® 2 FPGA System Planner Option
Allegro® ASIC Prototyping with FPGA’s
Cadence® SiP Layout – XL
Allegro® AMS Simulator1
Allegro® Pspice Systems Option
Allegro® PCB Symphony Team Design Option
OrbitIO